REMARKS

Initially, Applicants would like to express their appreciation of the courtesy extended by the Examiner in conducting a personal interview on August 3, 2001.

During the interview, the novelty and benefits of the present invention embodied in Claims 62-65 as amended above and new Claims 66-79 were discussed.

If there are any questions with regards to this preliminary amendment, the undersigned attorney can be contacted at the listed telephone number.

Respectfully submitted,

PRICE AND GESS

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

| 1 | 62. (Amended) A data processor performing data processing based on |
|----|---|
| 2 | an 8-bit instruction, comprising: |
| 3 | a plurality of registers; |
| 4 | a decoding unit decoding an 8-bit instruction, the instruction independently |
| 5 | designating: |
| 6 | one of a plurality of operations including transfer and calculation; |
| 7 | one of the plurality of registers as a source operand, and |
| 8 | one of the plurality of registers as a destination operand; |
| 9 | wherein [the plurality of registers includes at least one register] at least one |
| 10 | of the source operand register and the destination operand register is capable of |
| 11 | storing an address exceeding 16 bits; and |
| 12 | an execution unit for executing the decoded instruction. |
| 1 | 63. (Amended) A data processor performing data processing based on an 8- |
| 2 | bit instruction, comprising: |
| 3 | a plurality of registers; |
| 4 | a decoding unit decoding an 8-bit instruction, the instruction independently |
| 5 | designating: |
| 6 | one of a plurality of operations including transfer and calculation; |
| 7 | one of the plurality of registers as a source operand, and |
| 8 | one of the plurality of registers as a destination operand; |
| 9 | wherein at least one instruction is further followed by a [numeric code] |
| 10 | linear absolute address of more than 16 bits; and |
| 11 | an execution unit for executing the decoded instruction. |
| 1 | 64. (Amended) A data processor performing data processing based on an 8- |
| 2 | bit instruction, [the instruction independently designating: |
| 3 | one of a plurality of operations including transfer and calculation; |

| 4 | one of a plurality of registers as a source operand, and |
|----|--|
| 5 | one of the plurality of registers as a destination operand; |
| 6 | wherein a first register and a second register are included in the |
| 7 | plurality of registers, and |
| 8 | a judgement of which one of sign-extending and zero-extending is to be |
| 9 | performed on operand data is made depending on which of the first register and |
| 10 | the second register is designated as the destination operand in the instruction] |
| 11 | comprising: |
| 12 | a first register and a second register, |
| 13 | a decoding unit decoding an 8-bit instruction, |
| 14 | a judgment means for judging which one of sign-extending and zero- |
| 15 | extending is to be performed on operand data is made depending on which of the |
| 16 | first register and the second register is designated as the destination operand in the |
| 17 | instruction, and |
| 18 | an execution unit for executing the decoded instruction. |
| 1 | 65. (Amended) A data processor performing data processing based on |
| 2 | an 8-bit instruction, comprising: |
| 3 | a plurality of registers; |
| 4 | a decoding unit for decoding an 8-bit instruction, the instruction |
| 5 | independently designating: |
| 6 | one of a plurality of operations including transfer and calculation; |
| 7 | one of the plurality of registers as a source operand, and |
| 8 | one of the plurality of registers as a destination operand; |
| 9 | wherein an address register and a data register are included in the plurality |
| 10 | of registers, and |
| 11 | an address stored in the address register is longer than data stored in the |
| 12 | data register. |

New Claims 66-79 are submitted for examination on their merits.